



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,977	11/11/2003	Darrell Rinerson	P029.03.CIP14+D23	2976
42958	7590	07/26/2006	EXAMINER	
UNITY SEMICONDUCTOR CORPORATION 250 NORTH WOLFE ROAD SUNNYVALE, CA 94085			THOMAS, TONIAE M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/605,977

Applicant(s)

RINERSON ET AL.

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) 1-11 and 38-40 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 22-37 is/are allowed.
- 6) ☒ Claim(s) 13, 15 and 20 is/are rejected.
- 7) ☒ Claim(s) 14 and 16-19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office action is responsive to the amendment received on 09 May 2006.
2. Currently, claims 1-11, 14-20, and 22-40 are pending. Claims 1-11 and 38-40 have been withdrawn from further consideration.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 13, 15, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Doan et al. (US 6,150,253).

The Doan et al. patent (Doan) discloses a method of making an integrated circuit (see Figs. 1-15 and accompanying text). The method comprises: providing a semiconductor wafer 100 including active circuitry previously fabricated on the wafer (Fig. 1; col. 6, lines 25-30; and col. 6, lines 36-39); performing front end of line (FOEL) processes on the semiconductor wafer (see Figs. 5-9 and col. 6, line 63 - col. 7, line 42); forming a plurality of conductive memory devices (only one is shown) on the FEOL processed wafer and atop the active circuitry, each device being operable to be reversibly placed

in multiple resistive states (see Figs. 11-13 and col. 7, lines 45-55);¹ forming a sidewall layer 124 around the devices (Fig. 13 and col. 8, lines 33-36); and conducting metallization 126 after the devices are formed (fig. 15 and col. 8, lines 36-41).

The FEOL processes include the formation of a first inter-layer dielectric 116 (col. 7, lines 26-31).

A first metallization 102 is conducted before the memory devices are formed (Fig. 7 and col. 7, lines 3-9).

Allowable Subject Matter

4. Claims 14 and 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 22-37 are allowable over the prior art of record. The prior art of record does not anticipate, teach or suggest a method of making a plurality of conductive memory devices substantially as claimed, wherein the method comprises modifying an interface property between the multi-resistive state element layer and the top electrode.

Response to Arguments

5. Applicant's arguments filed 09 May 2006 have been fully considered but they are not persuasive.

¹ The memory devices comprise a chalcogenide layer of material, wherein the chalcogenide

6. Applicant argues that the Doan et al. reference (referred to hereinafter as Doan) does not teach providing a semiconductor wafer including active circuitry previously fabricated on the wafer. As stated above, Doan does disclose this limitation. See the rejection above. Accordingly, the rejection of claims 13, 15, and 20 under 35 USC 102(b) as made of record in the Office action mailed on 10 February 2006 is maintained in this Office action.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

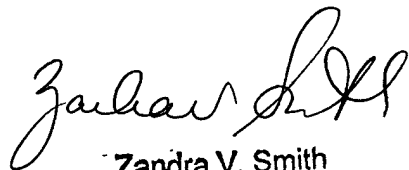
material can be reversibly placed in multiple resistive states.

Art Unit: 2822

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TMT
24 July 2006


Zandra V. Smith
Supervisory Patent Examiner
24 July 2006